Product Specification

425Gb/s DR4 OSFP 1310nm 500m
Optical Transceiver

P/N: 400G-OSFP-DR4

Features

- Hot Pluggable OSFP form factor
- Operating data rate 425Gbps
- Single +3.3V power supply
- MPO-12 APC connector
- Max power dissipation <10W
- Four Parallel 1310nm Optical Lanes
- 8*53.125Gbps (PAM4) Electrical Interface (400GAUI-8), 4*106.25Gbps (PAM4) Optical Interface (1*12 APC MPO)
- Up to 500m Transmission on Single Mode Fiber (SMF) with FEC
- PIN receivers
- Built-in digital diagnostic function
- Commercial temperature range 0°C to 70°C

Compliance

- Compliant with OSFP MSA
- Compliant with CMIS 5.1
- RoHS

Applications

- 400G Ethernet
- Cloud Services
- Data Center Interconnect
- Data center Enterprise networking
- Switches with OSFP ports

Description

The 400G-OSFP-DR4 is a cutting-edge silicon photonics (SiPh) transceiver module designed for high-speed, energy-efficient 400G data center interconnects. Leveraging an advanced SiPh platform, it integrates both active and passive optoelectronic components onto a single chip, delivering a cost-effective, low-power solution for 400GBASE-DR4 applications. Equipped with an MTP/MPO-12 connector, this module supports link lengths of up to 500 meters over single-mode fiber (SMF) and enables flexible deployment as a 1 x 400G connection or a 4 x 100G breakout via QSFP28-DR-100G modules.

Compliant with the OSFP Multi-Source Agreement (MSA), CMIS 4.0 I2C interface, and 400GAUI-8 standards, the 400G-OSFP-DR4 ensures robust interoperability and scalability in modern networks. It transmits 400 Gigabit Ethernet signals over four parallel 1310nm optical lanes, with one wavelength per lane, optimizing bandwidth efficiency and signal integrity. The innovative silicon photonics architecture reduces complexity and power consumption while maintaining high performance, making it ideal for next-generation hyperscale data centers.

Tailored for high-density, energy-conscious environments, this module excels in scenarios requiring extended reach and reliable 400G/100G connectivity. Its compact OSFP form factor, combined with silicon photonics' inherent advantages in integration and thermal management, supports seamless upgrades to 400G infrastructure. Whether deployed for spine-leaf architectures, AI/ML clusters, or storage networks, the 400G-OSFP-DR4 delivers future-proof agility and cost savings for demanding data center workloads.

Product performance Specifications

1. Basic Product Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Absolute Maximum Ratings					
Storage Temperature	T_S	-40	-	+85	°C
Operating Case Temperature	T_{OP}	0	-	70	°C
Power Supply Voltage	V_{CC}	-0.5	-	3.6	V
Relative Humidity (non condensing)	RH – Option 1	5		95	%
Control Input Voltage	V_I	-0.3	-	V_{CC}+0.5	V
Operational Specifications					
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Instantaneous peak current at hot plug (400G)	CC_IP	-	-	3600	mA
Sustained peak current at hot plug (400G)	ICC_SP	-	-	3000	mA
Maximum Power consumption (400G)	PD	-	-	9	W
Maximum Power consumption, Low Power Mode (400G)	PDLP	-	-	tbd	W
Instantaneous peak current at hot plug (200G)	ICC_IP	-	-	2200	mA
Sustained peak current at hot plug (200G)	ICC_SP	-	-	1840	mA

Maximum Power consumption (200G)	PD	-	-	5.5	W
Maximum Power consumption, Low Power Mode (200G)	PDLP	-	-	1.5	W
Signaling Rate per Lane	SRL	-	53.125	-	GBd

2. Product Optical and Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Pre FEC Bit Error Ratio				2.40E-04		
Post FEC Bit Error Ratio	Icc			1.00E-12		1
Transceiver						
Data rate per lane	DR		26.5625		GBd	
Modulation format			PAM4			
Center Wavelength	λ	1304.5	1310	1317.5	nm	
RMS spectral width	σ			0.6	nm	
Average Launch power, each lane	Pavg	-2.9		4	dBm	2
Outer Optical Modulation Amplitude (OMAouter), Each Lane	POMA	-0.8		4.2	dBm	3
Launch Power in OMAouter Minus TDECQ, Each Lane		-2.2			dB	
Transmitter and Dispersion Eye Clouser for PAM4, Each Lane	TDECQ			3.4	dB	4
Average Launch Power of OFF Transmitter, per Lane				-15	dBm	
Extinction ratio	ER	3.5			dB	
Transmitter power excursion, each lane				2.3	dBm	
Optical Return Loss Tolerance	ORLT			21.4	dB	
Transmitter Reflectance				-26	dBm	
Encircled fluxb		≥86% at 19 um ≤30% at 4.5 um				
Differential pk-pk Input Voltage tolerance	900				mV	5
Differential Termination Mismatch				10	%	
Differential Input Return Loss		IEEE802.3-2015Equation(83E-5)			dB	
Common-mode to differential-mode return loss		IEEE802.3ck Equation (120G–1)			dB	
Module Stressed Input Test		See IEEE 802.3bs 120E.3.4.1				6
Single-ended Voltage Tolerance Range(Min)		-0.4 to 3.3			V	
DC Common Mode Input Voltage		-350		2850	mV	7

RIN21.4OMA				-136	dB/Hz	
Receiver						
Data rate per lane	BR	26.5625±100ppm				Gbd
Modulation format		PAM4				
Center Wavelength	λ	1304.5	1310	1317.5	nm	
Damage threshold		5			dBm	8
Average receive power, each lane		-5.9		5	dBm	9
Receive power, each lane (OMAouter)				4.2	dBm	
Receiver reflectance	Rr			-26	dB	
Receiver Sensitivity(OMAouter), Each Lane		Equation(1)			dBm	10
Stressed receiver sensitivity, each lane				-1.9	dBm	11
Rx LOS	Assert		-15			dBm	
	De-assert				-8.9	dBm	
	Hysteresis		0.5			dB	
Differential Peak-to-Peak Output Voltage				900	mVpp	
Differential termination mismatch				10	%	
Eye height		15			mV	
Vertical eye closure				12	dB	
Common-mode to differential-mode return loss		IEEE802.3- 2015Equation(83E-3)				
Effective return loss		8.5			dB	
Transition time		9.5			ps	
Near-end Eye Symmetry Mask Width(ESMW)			0.265		UI	
Near-end Eye Height, Differential		70			mV	
Far-end Eye Symmetry Mask Width(ESMW)		0.2	0.2		UI	
Far-end Eye Height, Differential		30			mV	
Far-end Pre-cursor ISI Ratio		-4.5		2.5	%	
Common Mode Output Voltage(Vcm)		-350		2850	mV	
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test				3.4	dB	12

Note1: FEC is provided by host system.

Note2: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note3: Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1.1dB for an extinction ratio of < 5dB, the OMAOuter (min) must exceed the minimum value specified here.

Note4: Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement

Note5: With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

Note6: Meets BER specified in IEEE 802.3bs 120E.1.1.

Note7: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Note8: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note9: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power

Note10: Receiver sensitivity (OMAOuter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation (1), which is illustrated in Figure 1.

Note11: Measured with conformance test signal at TP3 for the BER equal to 2.4E-4.

Note12: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

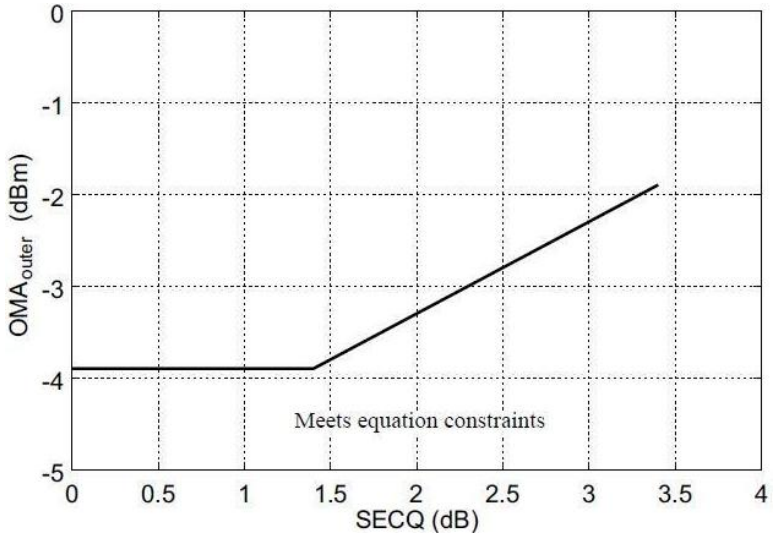


Figure 1. Illustration of Receiver Sensitivity Mask for 400G-DR4

= max(−3.9, − 5.3) (1) Where: RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

Recommended Host Board Power Supply Circuit

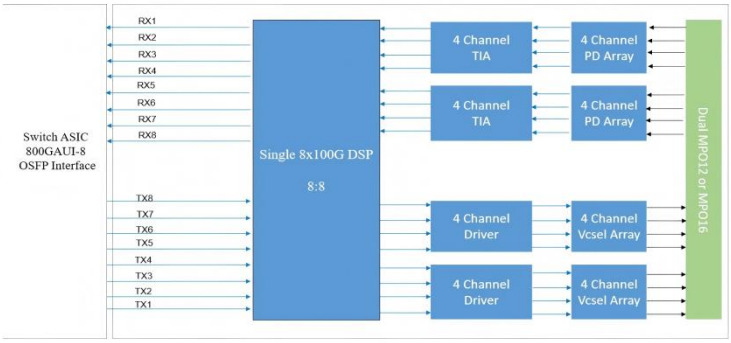


Figure 1: Module Block Diagram

Recommended Interface Circuit

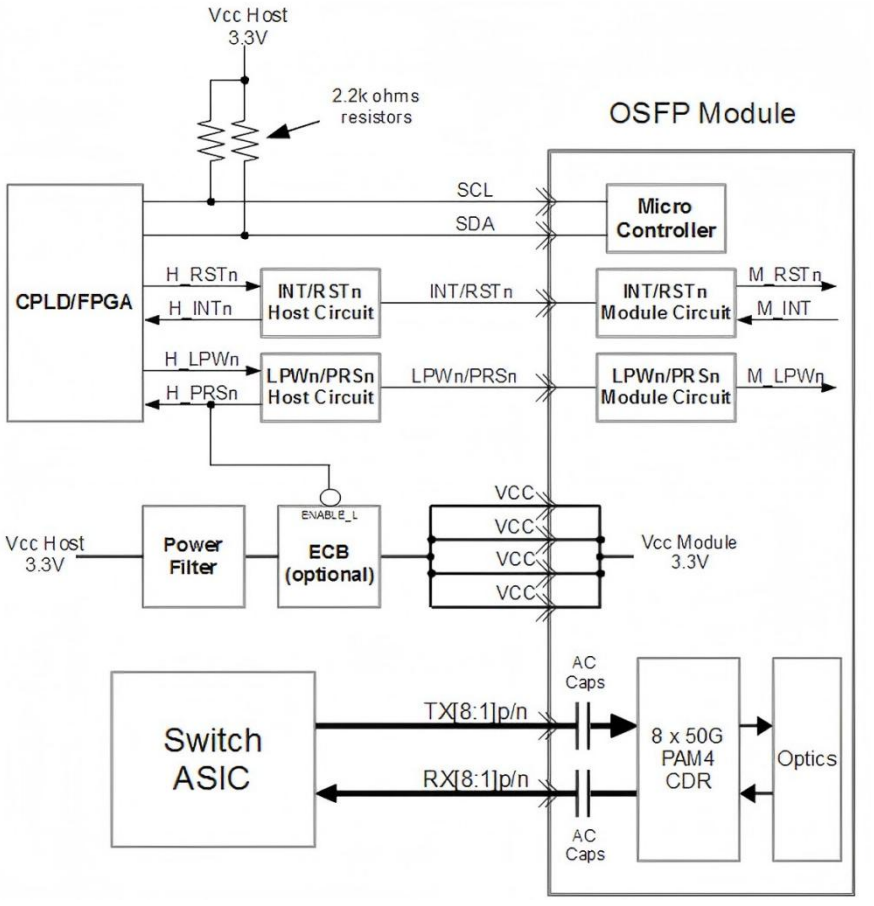


Figure2: Recommended Interface Circuit

Optical Interface

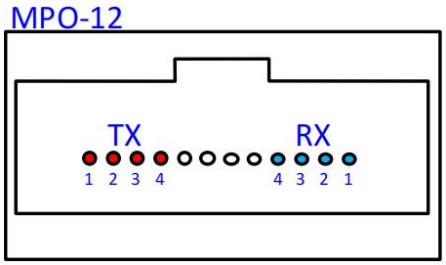


Figure3: Optical Lane Sequence

Pin-out Definition

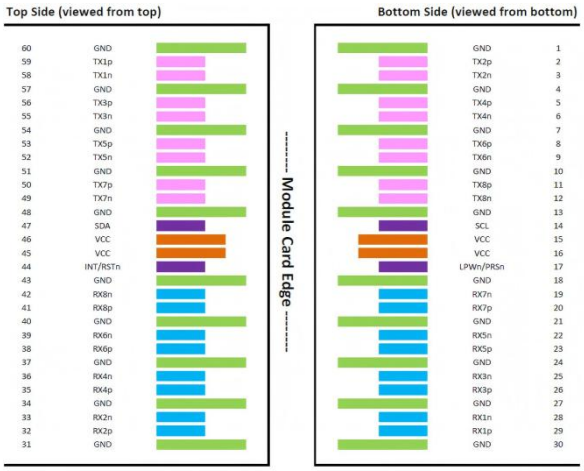


Figure4: Pin view

Pin Function Definitions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	

10		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	1
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	2
18		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	2
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	1

48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	
50	CML-I	TX7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	
59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Note1: Open-Drain with pull up resistor on Host.

Note2: See pin description for required circuit.

Monitoring Specification

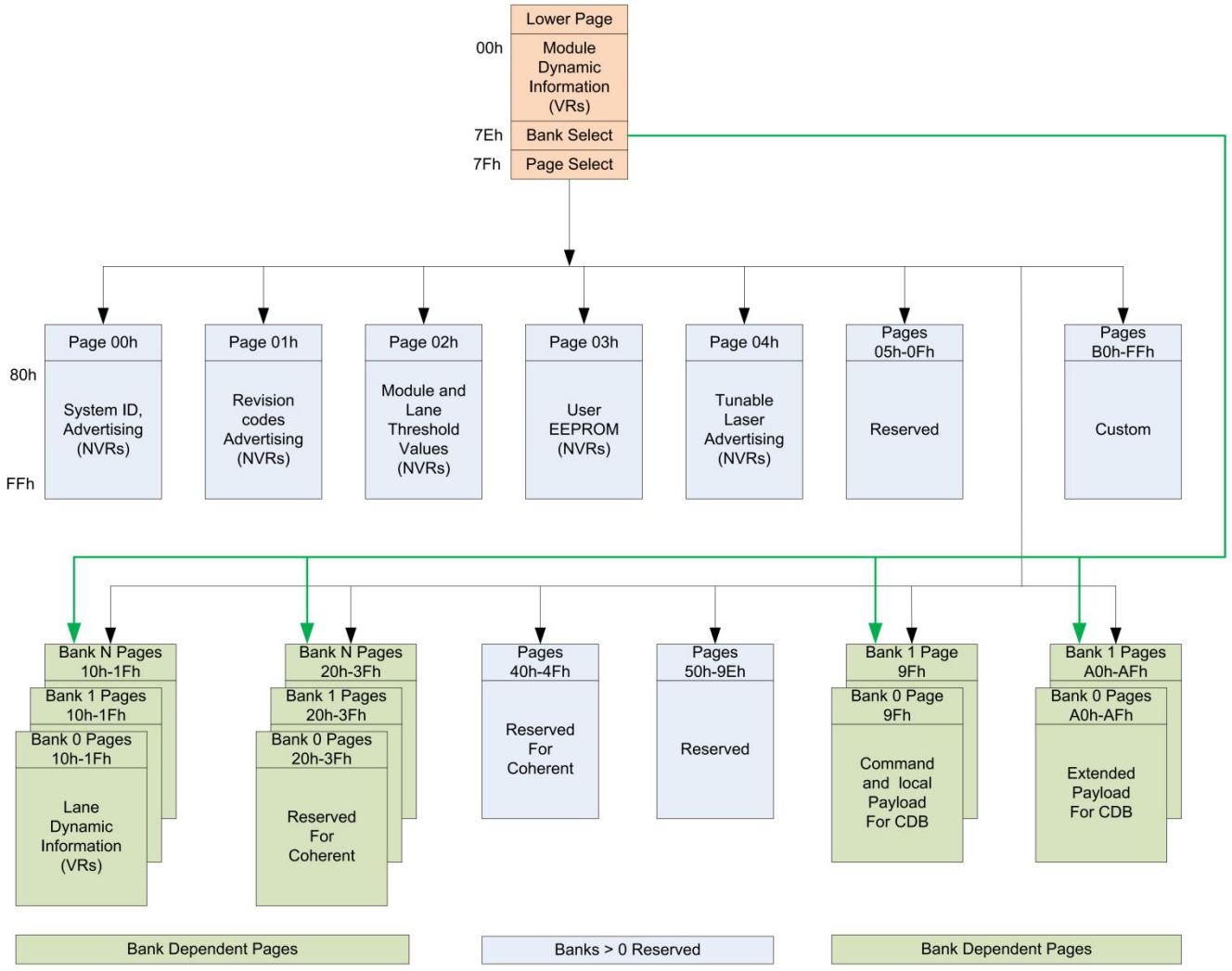


Figure5: Memory map

Memory map table

Byte	Unit	Name	Description
Lower Page 00h			
0	1	Identifier	Identifier - Type of Serial Module - See SFF-8024.
1	1	Revision Compliance	Identifier – CMIS revision; the upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.
2-3	2	ID and Status Area	Flat mem indication, CLEI present indicator, Maximum TWI speed,

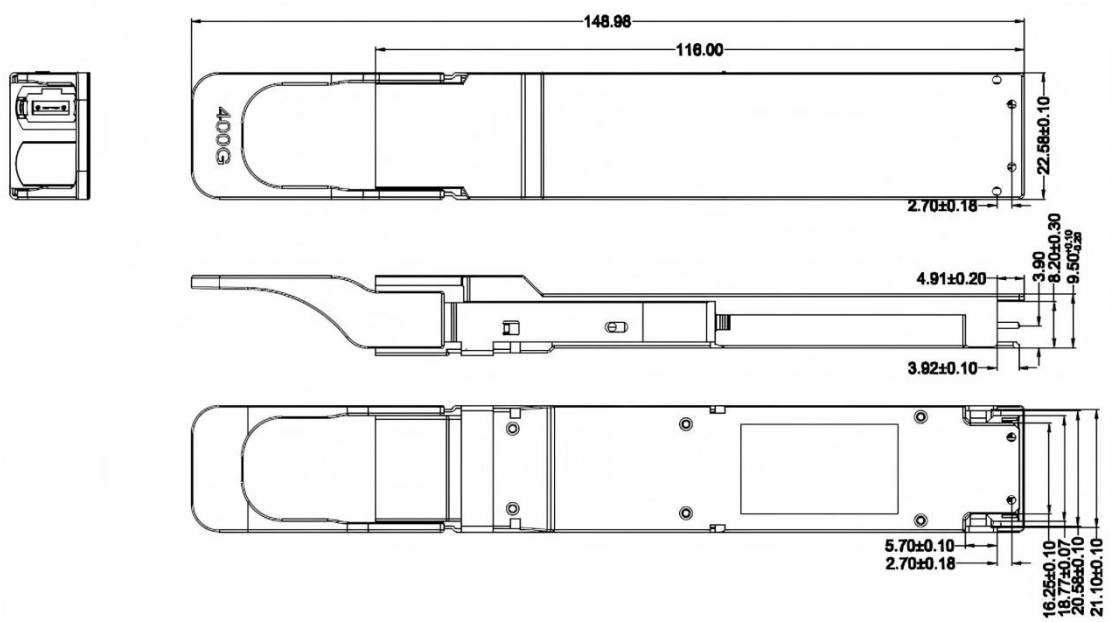
			Current state of Module, Current state of the Interrupt signal.
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh.
8-13	6	Module-Level Flags	All flags that are not lane or data path specific.
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific.
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	Password Entry and Change
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page
Upper Page 00h			
128	1	Identifier	Identifier - Type of Serial Module - See SFF-8024.
129-144	16	Vendor name	Vendor name (ASCII)
145-147	2	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	8	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	10	Vendor SN	Vendor Serial Number (ASCII)
182-183	2	Date code year	ASCII code, two low order digits of year (00=2000)
184-185	2	Date code month	ASCII code digits of month (01=Jan through 12=Dec)
186-187	2	Date code day of month	ASCII code day of month (01-31)
188-189	2	Lot code	ASCII code, custom lot code, may be blank
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	Module power characteristics
202	1	Cable assembly length	Cable assembly length
203	1	Media Connector Type	Media Connector Type
204	1	5 GHz attenuation	Passive copper cable attenuation at 5 GHz in 1 dB increments
205	1	7 GHz attenuation	Passive copper cable attenuation at 7 GHz in 1 dB increments
206	1	12.9 GHz attenuation	Passive copper cable attenuation at 12.9 GHz in 1 dB increments
207	1	25.8 GHz attenuation	Passive copper cable attenuation at 25.8 GHz in 1 dB increments
208-209	2	Reserved	Reserved
210-211	2	Cable Assembly Lane Information	Cable Assembly Lane Information

212	1	Media Interface Technology	Media Interface Technology
213-220	8	Reserved	Reserved
221	1	Custom	Custom
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	Custom Info NV
Page 01h (Optional)			
128	1	Inactive Module firmware major revision	Numeric representation of inactive module firmware major revision
129	1	Inactive Module firmware minor revision	Inactive Module firmware minor revision
130	1	Module hardware major revision	Module hardware major revision
131	1	Module hardware minor revision	Module hardware minor revision
132	1	Length (SMF)	Bits7-6 Length multiplier(SMF),Bits 5-0 Base Length (SMF)
133	1	Length (OM5)	Link length supported for OM5 fiber, units of 2 m (2 to 510 m)
134	1	Length (OM4)	Link length supported for OM4 fiber, units of 2 m (2 to 510 m)
135	1	Length (OM3)	Link length supported for EBW 50/125 μm fiber (OM3), units of 2m (2 to 510 m)
136	1	Length (OM2)	Link length supported for 50/125 μm fiber (OM2), units of 1m (1 to 255 m)
137	1	Reserved	Reserved
138-139	2	Nominal Wavelength	Nominal Wavelength
140-141	2	Wavelength Tolerance	Wavelength Tolerance
142-144	3	Implemented Memory Pages and Durations advertising	Implemented Memory Pages and Durations advertising
145-154	10	Module Characteristics advertising	Module Characteristics advertising
155-156	2	Implemented Controls advertising	Implemented Controls advertising
157-158	2	Implemented Flags advertising	Implemented Flags advertising
159-160	2	Implemented Monitors advertising	Implemented Monitors advertising
161-162	2	Implemented Signal Integrity Controls advertising	Implemented Signal Integrity Controls advertising
163-166	4	CDB support advertising	CDB support advertising
167-168	2	Additional Durations advertising	Additional Durations advertising
169-175	7	Reserved	Reserved
176-190	15	Module Media Lane advertising	Coded 1 if the Application is allowed to begin on a given media lane. Bits 0-7 correspond to Host Lanes 1-8. In multi-lane Applications each instance of an Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised,

			all instance must be supported concurrently.
191-222	32	Custom	Custom
223-250	28	Extended Module Host-Media Interface Advertising options	Extended Module Host-Media Interface Advertising options
251-254	4	Reserved	Reserved
255	1	Checksum	Checksum
Page 02h (Optional)			
128-129	2	Temperature monitor high alarm	Thresholds for internally measured temperature monitor: signed 2's complement in 1/256 degree Celsius increments
130-131	2	Temperature monitor low alarm	
132-133	2	Temperature monitor high warning	
134-135	2	Temperature monitor low warning	
136-137	2	Supply 3.3-volt monitor high alarm	Thresholds for internally measured 3.3 volt input supply voltage: in 100 µV increments
138-139	2	Supply 3.3-volt monitor low alarm	
140-141	2	Supply 3.3-volt monitor high warning	
142-143	2	Supply 3.3-volt monitor low warning	
144-145	2	Aux 1 monitor high alarm	Thresholds for TEC Current or Reserved monitor TEC Current: signed 2's complement in 100/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling
146-147	2	Aux 1 monitor low alarm	
148-149	2	Aux 1 monitor high warning	
150-151	2	Aux 1 monitor low warning	
152-153	2	Aux 2 monitor high alarm	Thresholds for TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 100/32767%increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2's complement in 1/256 degree Celsius increments
154-155	2	Aux 2 monitor low alarm	
156-157	2	Aux 2 monitor high warning	
158-159	2	Aux 2 monitor low warning	
160-161	2	Aux 3 monitor high alarm	Thresholds for Laser Temperature or additional supply voltage monitorLaser Temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Laser Temp can be below 0 if uncooled or in Tx Disable.Additional supply voltage monitor: in 100 µV increments
162-163	2	Aux 3 monitor low alarm	
164-165	2	Aux 3 monitor high warning	
166-167	2	Aux 3 monitor low warning	
168-169	2	Custom monitor high alarm	Custom monitor: signed or unsigned 16 bit value
170-171	2	Custom monitor low alarm	
172-173	2	Custom monitor high warning	
174-175	2	Custom monitor low warning	

176-177	2	Tx optical power high alarm	Threshold for Tx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)See section 8.8.3 for monitor details including accuracy
178-179	2	Tx optical power low alarm	
180-181	2	Tx optical power high warning	
182-183	2	Tx optical power low warning	
184-185	2	Tx bias current high alarm	Threshold for Tx bias monitor: unsigned integer in 2 uA increments, times the multiplier from Table 8-33. See section 8.8.3 for monitor details including accuracy
186-187	2	Tx bias current low alarm	
188-189	2	Tx bias current high warning	
190-191	2	Tx bias current low warning	
192-193	2	Rx optical power high alarm	Threshold for Rx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 8.8.3 for accuracy.
194-195	2	Rx bias current low alarm	
196-197	2	Rx bias current high warning	
198-199	2	Rx bias current low warning	
200-229	30	Reserved	Reserved
230-254	25	Custom	Custom
255	1	Checksum	Covers bytes 128-254

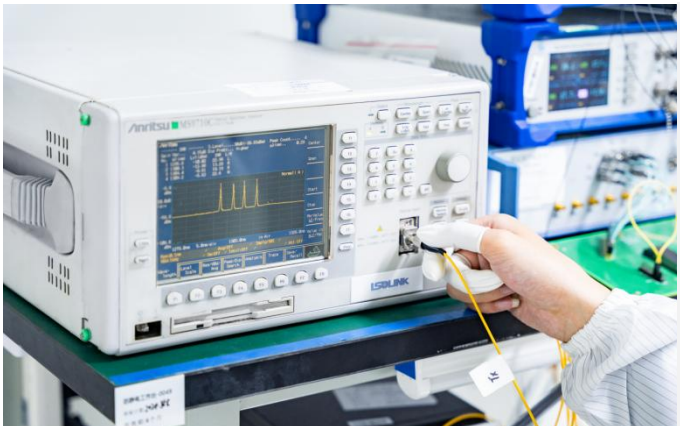
Mechanical Dimension



Test Center

1. Performance Testing

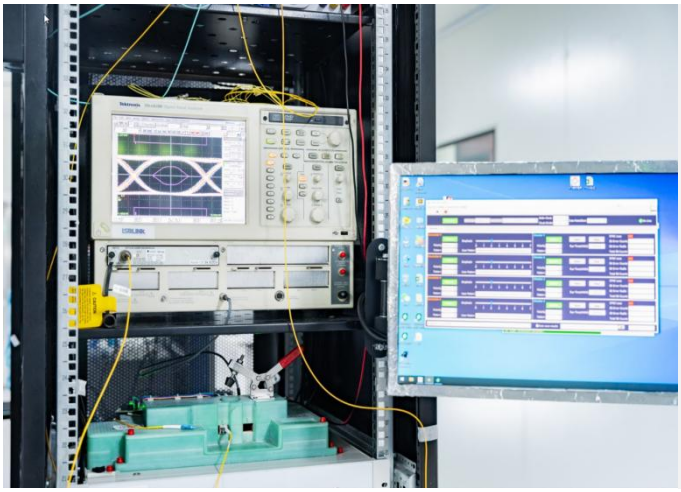
Every fiber optic transceiver is thoroughly tested by the LSOLINK Assurance Program, which is equipped with the world's most advanced analytical equipment to ensure that our transceivers meet the industry's international public protocol standards while still functioning flawlessly in your facility.



Optical Spectrum Inspection

Using the industry's leading optical spectrum analyser to check in real time that the parameters of the optical transceiver's laser comply with industry standards.

- **Peak:** Peak wavelength and peak level
- **2nd Peak:** Side-mode wavelength and level
- **Mean WI:** Center wavelength
- **Total Power:** Total power of spectrum
- **SMSR:** Side-Mode Suppression Ratio



Optical Signal Quality Inspection

Using highly efficient sampling oscilloscopes and BERT testers, equipped with an automated test platform to accurately test the signal quality of the transceiver, test records are kept for up to 5 years to ensure the traceability of each transceiver.

- **Eye Mask Margin(NRZ)**
- **TDECQ(PAM4):**transmitter dispersion eye closure
- **OMA:** Optical modulation amplitude
- **BER:** Bit error rate
- **ER:** Extinction Ratio

Flow Pressure Test

Using multi-protocol network traffic analyser with various brands of switches to test the transceiver's ability to transmit at full speed.

- **Bandwidth:** Actual transceiver bandwidth on the port
- **Packet Loss**
- **Packet Errors:**CRC Errors/PCS Errors/Symbol Errors
- **LinkDown Counts**
- **latency**

Aboveis part of our test bed network equipment. For more information, Please click download for optical transceiver performance test report.

2. Quality Control

We adopt advanced quality management solutions. Each transceiver is self-inspected, including:20x microscope inspection, 200x microscope inspection, and QC process inspection.

visual inspection

Microscopic inspection: 20X

Microscopic inspection: 200X

Reliability Verification

Optical endface inspection

OQC Inspection

Order Information

Part Number	Description
400G-OSFP-VR4	400GBASE-VR4 OSFP PAM4 850nm 50m DOM MTP/MPO-12 APC MMF Transceiver Module，Flat Top
400G-OSFP-SR4	400GBASE-SR4 OSFP PAM4 850nm 100m DOM MTP/MPO-12 APC MMF Optical Transceiver Module
400G-OSFP-DR4	400GBASE-DR4 OSFP PAM4 1310nm 500m DOM MTP/MPO-12 APC SMF Optical Transceiver Module
800G-OSFP-2VR4	800GBASE-2xSR4 OSFP PAM4 850nm 50m DOM Dual MTP/MPO-12 APC MMF Optical Transceiver Module
800G-OSFP-2SR4	800GBASE-2xSR4 OSFP PAM4 850nm 100m DOM Dual MTP/MPO-12 APC MMF Optical Transceiver Module
800G-OSFP-2DR4	800GBASE-2xDR4 OSFP PAM4 1310nm 500m DOM Dual MTP/MPO-12 APC SMF Optical Transceiver Module
800G-OSFP-2FR4	800GBASE-2xFR4 OSFP PAM4 1310nm 2km DOM Dual Duplex LC SMF Optical Transceiver Module

Further Information

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Disclaimer

1. We are committed to continuous product improvement and feature upgrades, and the contents con t ained in this manual are subject to change without notice.
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