

Features

- Supporting 200Gbps to 2x100Gbps
- Available length range 1m~100m
- Active Optical Cable
- Operating data rate 212.5Gbps
- Single +3.3V power supply
- Max power dissipation <4.5W
- VCSEL Array Transmitter and PIN Array Receiver
- High-Density QSFP56 38-PIN and 4x SFP56 20-PIN
 Connector
- 4-Channel Full-Duplex Active Optical Cable
- Commercial temperature range 0°C to 70°C

Compliance

- Compliant with SFP56 MSA
- Compliant with Electrical MSA SFF-8636
- Compliant with Mechanical MSA SFF-8665
- IEEE 802.3bj
- RoHS

Applications

- Supports InfiniBand HDR/EDR Systems
- Switches, servers, routers and HBA
- Data center cabling infrastructure
- High speed multi-channel parallel data connections



Description

The HDR-Q56-2Q-A is an breakout active optical cable (AOC) designed to support InfiniBand HDR 200G on one end, with two 100G EDR 100G connections on the other. Featuring QSFP56 connectors, this cable enables the efficient bifurcation of a single 200G link into two 100G connections, making it a versatile solution for high-performance data transmission in demanding environments such as data centers and supercomputing applications.

The HDR-Q56-2Q-A cable is ideal for applications where multiple lower-bandwidth connections are required from a single high-bandwidth source. It ensures high-speed, low-latency data transfer while maintaining excellent signal integrity, making it suitable for high-performance computing, artificial intelligence, and large-scale cloud infrastructure. Its AOC design reduces power consumption and supports long-distance transmission, while the passive nature of the cable ensures reliable and cost-effective performance in dense, high-bandwidth network configurations.

Product performance Specifications

1. Basic Product Characteristics

Parameter	Symbol	Min	Тур.	Max	Unit			
Absolute Maximum Ratings								
Supply voltage	V _{CC}	-0.3	-	3.6	V			
Data input voltage		-0.3	-	3.465	V			
Control input voltage	Vı	-0.3	-	4.0	V			
Damage threshold		3.4	-	-	dBm			
Storage temperature	Ts	-40	-	85	°C			
	Operational Spec	ifications						
Supply Voltage	Vcc	3.135	-	3.465	V			
Power dissipation (200G re-timing on all lanes)		-	4.35	4.55	W			
Power dissipation (100G re-timing on all lanes)		-	2.5	2.75	W			
Supply noise tolerance (10Hz-10MHz)		66	-	-	mVpp			
Operating case temperature	T _{oc}	0	-	70	°C			
Operating relative humidity	RH	5	-	85	%			



2. Product Optical and Electrical Characteristics

Parameter	Symbol	Min	Тур.	Max	Unit	Note	
Transmitter							
Signaling Speed per Lane		PRBS31Q@26.5625Gbd PAM4			Gb/s		
Differential Input Impedance	Z _{IN}	90	100	110	Ω		
Center Wavelength	С	840	850	860	nm		
Differential Input Voltage	V_{IN}	-	900	-	mVpp		
Differential termination mismatch				10	%		
DC common mode voltage		350		2850	mV		
		Receiver					
Signaling Speed per Lane		PRBS3	1Q@26.5625Gb	od PAM4	Gb/s		
Center Wavelength	С	840	850	860	nm		
Differential Input Impedance				10	%		
Differential Input Voltage	Zout	90	100	110	Ω		
Differential termination mismatch	Vout			900	mVpp		
DC common mode voltage		-350		2850	mV		
Error Bit Rate	BER			2.4E-4			

Note1: PRBS31Q@26.5625Gbd PAM4



Recommended Host Board Power Supply Circuit

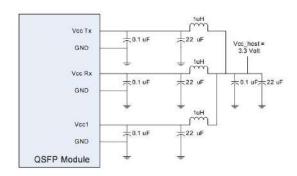


Figure 1:Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

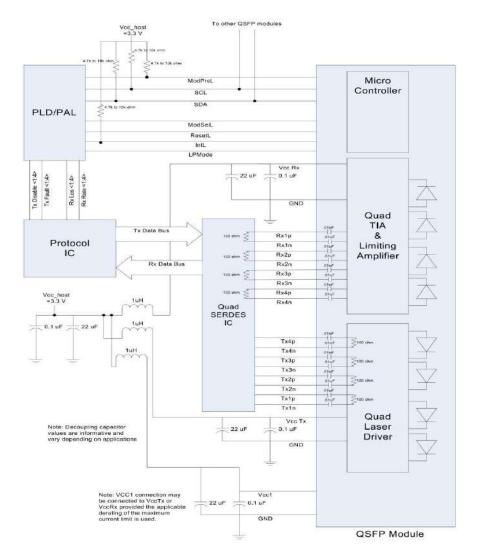


Figure2:Recommended Interface Circuit



Pin-out Definition

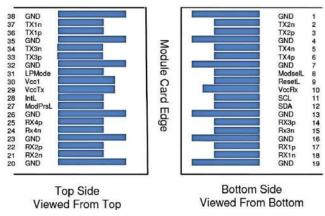


Figure3:Pin view

Pin Function Definitions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	4
9	LVTTL-I	ReSelL	Module Select	4
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	4
12	LVCMOS-I/O	SDA	2-wire serial interface data	4
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3



25	CML-O	Rx4p	Receiver Non-Inverted Data Output Ground	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	4
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	4
32		GND	Ground	1
33	CML-I	Тх3р	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3
38		GND	Ground	1

Note1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Note3: High-speed signal interfaces require differential pairs (e.g. TX1+/TX1-) with tightly matched impedances (typically 100Ω).

Note4: The management and control signals are based on LVTTL level logic and are used for functions such as module selection and reset.



Monitoring Specification

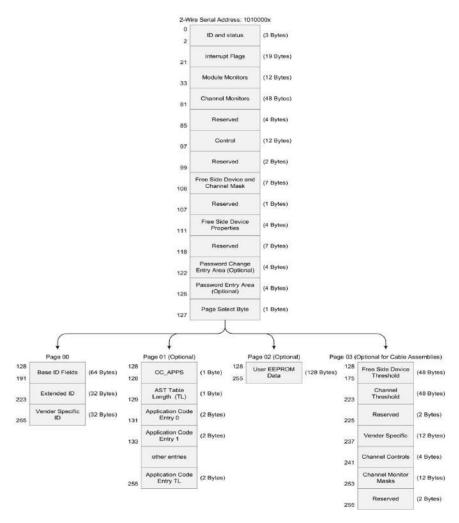


Figure4:QSFP Memory map

Memory map Table

Byte	Unit	Name	Description				
	Lower Page 00h						
0	1	Identifier	Type of transceiver,Page 00h Byte 0 and Page 00h Byte 128 shall contain the same parameter values.				
1	1	Status	Revision Compliance				
2	1	Status	Status indicators				
3-21	19	Interrupt Flags	Consist of interrupt flags for LOS, Tx Fault, warnings and alarms. The non-asserted state shall be 0b.				
22	1	Temperature MSB	Internally measured temperature (MSB)				
23	1	Temperature LSB	Internally measured temperature (LSB)				
24-25	2	Reserved	Reserved				



1	26	1	Supply Voltage MSB	Internally measured supply voltage (MSB)
28-29 2 Reserved Reserved				
30-33				
1				
1				volidor opositio
36 1 Rx2 Power MSB Internally measured Rx2 input power 37 1 Rx2 Power LSB Internally measured Rx2 input power 38 1 Rx3 Power MSB Internally measured Rx3 input power 40 1 Rx4 Power LSB Internally measured Rx4 input power 41 1 Rx4 Power LSB Internally measured Rx4 input power 41 1 Rx4 Power LSB Internally measured Rx4 input power 42 1 Tx1 Bias LSB Internally measured Tx1 bias 43 1 Tx1 Bias LSB Internally measured Tx2 bias 45 1 Tx2 Bias LSB Internally measured Tx3 bias 46 1 Tx3 Bias LSB Internally measured Tx4 bias 47 1 Tx3 Bias LSB Internally measured Tx4 bias 48 1 Tx4 Bias LSB Internally measured Tx1 Power 50 1 Tx1 Power MSB Internally measured Tx2 Power 51 1 Tx1 Power LSB Internally measured Tx2 Power 53 1 Tx2 Power MSB Internally measured Tx3				Internally measured Rx1 input power
37 1 Rx2 Power LSB Internally measured Rx2 input power 38 1 Rx3 Power MSB Internally measured Rx3 input power 40 1 Rx4 Power LSB Internally measured Rx4 input power 41 1 Rx4 Power LSB Internally measured Rx4 input power 41 1 Rx4 Power LSB Internally measured Tx1 bias 42 1 Tx1 Bias MSB Internally measured Tx2 bias 43 1 Tx2 Bias LSB Internally measured Tx2 bias 45 1 Tx2 Bias LSB Internally measured Tx3 bias 46 1 Tx3 Bias MSB Internally measured Tx4 bias 47 1 Tx3 Bias LSB Internally measured Tx4 bias 48 1 Tx4 Bias LSB Internally measured Tx4 Dower 50 1 Tx1 Power LSB Internally measured Tx1 Power 51 1 Tx1 Power LSB Internally measured Tx2 Power 53 1 Tx2 Power LSB Internally measured Tx3 Power 56 1 Tx3 Power LSB Internally measured Tx4 Power				
38 1 Rx3 Power MSB Internally measured Rx3 input power 39 1 Rx3 Power MSB Internally measured Rx4 input power 40 1 Rx4 Power MSB Internally measured Rx4 input power 41 1 Rx4 Power LSB Internally measured Tx1 bias 42 1 Tx1 Bias MSB Internally measured Tx1 bias 43 1 Tx2 Bias LSB Internally measured Tx2 bias 45 1 Tx2 Bias LSB Internally measured Tx3 bias 46 1 Tx3 Bias MSB Internally measured Tx4 bias 47 1 Tx3 Bias LSB Internally measured Tx4 bias 48 1 Tx4 Bias LSB Internally measured Tx1 Power 49 1 Tx4 Bias LSB Internally measured Tx1 Power 50 1 Tx1 Power MSB Internally measured Tx2 Power 51 1 Tx2 Power MSB Internally measured Tx3 Power 53 1 Tx2 Power MSB Internally measured Tx3 Power 55 1 Tx3 Power LSB Internally measured Tx4 Power				Internally measured Rx2 input power
1				
1				Internally measured Rx3 input power
1				
42 1 Tx1 Bias MSB Internally measured Tx1 bias 43 1 Tx1 Bias LSB Internally measured Tx1 bias 44 1 Tx2 Bias LSB Internally measured Tx2 bias 45 1 Tx2 Bias LSB Internally measured Tx3 bias 46 1 Tx3 Bias MSB Internally measured Tx3 bias 47 1 Tx3 Bias MSB Internally measured Tx4 bias 48 1 Tx4 Bias LSB Internally measured Tx4 bias 50 1 Tx4 Power MSB Internally measured Tx1 Power 51 1 Tx1 Power LSB Internally measured Tx2 Power 52 1 Tx2 Power MSB Internally measured Tx2 Power 53 1 Tx2 Power MSB Internally measured Tx3 Power 54 1 Tx3 Power MSB Internally measured Tx4 Power 55 1 Tx4 Power MSB Internally measured Tx4 Power 66 1 Tx4 Power MSB Internally measured Tx4 Power 58-65 8 Reserved Reserved dannel monitor set 4 <td< td=""><td></td><td></td><td></td><td>Internally measured Rx4 input power</td></td<>				Internally measured Rx4 input power
1		1	Tx1 Bias MSB	
44 1 Tx2 Bias MSB Internally measured Tx2 bias 45 1 Tx3 Bias LSB Internally measured Tx3 bias 46 1 Tx3 Bias LSB Internally measured Tx3 bias 47 1 Tx3 Bias LSB Internally measured Tx4 bias 48 1 Tx4 Bias LSB Internally measured Tx4 bias 50 1 Tx1 Power MSB Internally measured Tx1 Power 51 1 Tx2 Power MSB Internally measured Tx2 Power 52 1 Tx2 Power MSB Internally measured Tx2 Power 53 1 Tx2 Power MSB Internally measured Tx3 Power 54 1 Tx3 Power LSB Internally measured Tx4 Power 55 1 Tx3 Power LSB Internally measured Tx4 Power 56 1 Tx4 Power MSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved 8c-99				Internally measured Tx1 bias
1		1		
46 1 Tx3 Bias MSB Internally measured Tx3 bias 47 1 Tx3 Bias LSB Internally measured Tx4 bias 48 1 Tx4 Bias MSB Internally measured Tx4 bias 49 1 Tx4 Bias LSB Internally measured Tx4 bias 50 1 Tx1 Power MSB Internally measured Tx1 Power 51 1 Tx2 Power MSB Internally measured Tx2 Power 53 1 Tx2 Power LSB Internally measured Tx3 Power 54 1 Tx3 Power LSB Internally measured Tx4 Power 55 1 Tx4 Power MSB Internally measured Tx4 Power 56 1 Tx4 Power LSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific 82-85 4 Reserved Reserved 100-106		1		Internally measured Tx2 bias
47 1 Tx3 Bias LSB Internally measured Tx3 bias 48 1 Tx4 Bias MSB Internally measured Tx4 bias 49 1 Tx4 Bias LSB Internally measured Tx4 bias 50 1 Tx1 Power MSB Internally measured Tx1 Power 51 1 Tx1 Power LSB Internally measured Tx2 Power 52 1 Tx2 Power LSB Internally measured Tx2 Power 53 1 Tx2 Power LSB Internally measured Tx3 Power 54 1 Tx3 Power LSB Internally measured Tx3 Power 55 1 Tx4 Power MSB Internally measured Tx3 Power 56 1 Tx4 Power LSB Internally measured Tx3 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx3 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific				
48 1 Tx4 Bias MSB Internally measured Tx4 bias 49 1 Tx4 Bias LSB Internally measured Tx4 bias 50 1 Tx1 Power MSB Internally measured Tx1 Power 51 1 Tx1 Power LSB Internally measured Tx2 Power 52 1 Tx2 Power LSB Internally measured Tx2 Power 53 1 Tx2 Power LSB Internally measured Tx3 Power 54 1 Tx3 Power LSB Internally measured Tx4 Power 55 1 Tx4 Power LSB Internally measured Tx4 Power 56 1 Tx4 Power LSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free		1		Internally measured Tx3 bias
1				
50 1 Tx1 Power MSB Internally measured Tx1 Power 51 1 Tx1 Power LSB Internally measured Tx2 Power 52 1 Tx2 Power MSB Internally measured Tx2 Power 53 1 Tx2 Power LSB Internally measured Tx3 Power 54 1 Tx3 Power LSB Internally measured Tx3 Power 55 1 Tx4 Power MSB Internally measured Tx4 Power 56 1 Tx4 Power LSB Internally measured Tx3 Power 57 1 Tx4 Power MSB Internally measured Tx3 Power 58 1 Tx4 Power LSB Internally measured Tx2 Power 17 1 Tx4 Power LSB Internally measured Tx2 Power 1 1 Tx4 Power LSB Internally measured Tx2 Power Internally measured Tx2 Power Internally measured Tx2 Power 1 Tx4 Power LSB Internally measured Tx3 Power Internally measured Tx3 Power Internally measured Tx3 Power Internally measured Tx3 Power Internally measured Tx3 Power 56 1 Tx4 Power LSB <	49	1		Internally measured Tx4 bias
51 1 Tx1 Power LSB 52 1 Tx2 Power MSB Internally measured Tx2 Power 53 1 Tx2 Power LSB Internally measured Tx3 Power 54 1 Tx3 Power MSB Internally measured Tx3 Power 55 1 Tx4 Power MSB Internally measured Tx4 Power 56 1 Tx4 Power LSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks Free Side Device Properties 107-110 4 Free Side Device Properties - The PCI Express External Cable Specification 111-112 2 Assigned for use by PCI Express - The PCI Express OCuLink Specification 113-117 4 </td <td>50</td> <td>1</td> <td>Tx1 Power MSB</td> <td></td>	50	1	Tx1 Power MSB	
53 1 Tx2 Power LSB Internally measured Tx2 Power 54 1 Tx3 Power MSB Internally measured Tx3 Power 55 1 Tx3 Power LSB Internally measured Tx4 Power 56 1 Tx4 Power LSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks Free Side Device Properties 107-110 4 Free Side Device Properties Used for:	51	1	Tx1 Power LSB	Internally measured Tx1 Power
53 1 Tx2 Power LSB 54 1 Tx3 Power MSB Internally measured Tx3 Power 55 1 Tx3 Power LSB Internally measured Tx4 Power 56 1 Tx4 Power LSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks Free Side Device Properties 107-110 4 Free Side Device Properties - The PCI Express External Cable Specification 111-112 2 Assigned for use by PCI Express - The PCI Express OCuLink Specification 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved	52	1	Tx2 Power MSB	
55 1 Tx3 Power LSB Internally measured Tx3 Power 56 1 Tx4 Power MSB Internally measured Tx4 Power 57 1 Tx4 Power LSB Internally measured Tx4 Power 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks 107-110 4 Free Side Device Properties Free Side Device Properties 111-112 2 Assigned for use by PCI Express - The PCI Express External Cable Specification 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved	53	1	Tx2 Power LSB	Internally measured Tx2 Power
55 1 Tx3 Power LSB 56 1 Tx4 Power MSB 57 1 Tx4 Power LSB 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks 107-110 4 Free Side Device Properties Free Side Device Properties 111-112 2 Assigned for use by PCI Express Used Tree Side Device Properties 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved 118 Reserved Reserved 118 Reserved Reserved Channel Manual Masks 107-100 Control 113-117 A Free Side Device Properties Free Side Device Properties 118 Reserved Reserved	54	1	Tx3 Power MSB	
Tx4 Power LSB Internally measured Tx4 Power	55	1	Tx3 Power LSB	Internally measured 1x3 Power
57 1 Tx4 Power LSB 58-65 8 Reserved Reserved channel monitor set 4 66-73 8 Reserved Reserved channel monitor set 5 74-81 8 Vendor Specific Vendor Specific 82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks 107-110 4 Free Side Device Properties Free Side Device Properties 111-112 2 Assigned for use by PCI Express - The PCI Express External Cable Specification - The PCI Express OCuLink Specification 113-117 4 Free Side Device Properties Reserved	56	1	Tx4 Power MSB	
66-738ReservedReserved channel monitor set 574-818Vendor SpecificVendor Specific82-854ReservedReserved86-9914ControlControl100-1067Free Side Device and Channel MasksFree Side Device and Channel Masks107-1104Free Side Device PropertiesFree Side Device Properties111-1122Assigned for use by PCI Express- The PCI Express External Cable Specification113-1174Free Side Device PropertiesFree Side Device Properties1181ReservedReserved	57	1	Tx4 Power LSB	Internally measured 1x4 Power
74-818Vendor SpecificVendor Specific82-854ReservedReserved86-9914ControlControl100-1067Free Side Device and Channel MasksFree Side Device and Channel Masks107-1104Free Side Device PropertiesFree Side Device Properties111-1122Assigned for use by PCI Express- The PCI Express External Cable Specification - The PCI Express OCuLink Specification113-1174Free Side Device PropertiesFree Side Device Properties1181Reserved	58-65	8	Reserved	Reserved channel monitor set 4
82-85 4 Reserved Reserved 86-99 14 Control Control 100-106 7 Free Side Device and Channel Masks 107-110 4 Free Side Device Properties Free Side Device Properties Used for: 111-112 2 Assigned for use by PCI Express - The PCI Express External Cable Specification - The PCI Express OCuLink Specification 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved	66-73	8	Reserved	Reserved channel monitor set 5
86-9914ControlControl100-1067Free Side Device and Channel MasksFree Side Device and Channel Masks107-1104Free Side Device PropertiesFree Side Device Properties111-1122Assigned for use by PCI Express- The PCI Express External Cable Specification113-1174Free Side Device PropertiesFree Side Device Properties1181ReservedReserved	74-81	8	Vendor Specific	Vendor Specific
Free Side Device and Channel Masks Free Side Device and Channel Masks Free Side Device Properties Free Side Device Properties Used for: The PCI Express External Cable Specification The PCI Express OCuLink Specification Free Side Device Properties Reserved Reserved	82-85	4	Reserved	Reserved
100-106 7 Masks Free Side Device and Channel Masks 107-110 4 Free Side Device Properties Free Side Device Properties Used for: 111-112 2 Assigned for use by PCI Express - The PCI Express External Cable Specification - The PCI Express OCuLink Specification 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved	86-99	14	Control	Control
Used for: 111-112 2 Assigned for use by PCI Express - The PCI Express External Cable Specification - The PCI Express OCuLink Specification 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved	100-106	7		Free Side Device and Channel Masks
111-112 2 Assigned for use by PCI Express - The PCI Express External Cable Specification - The PCI Express OCuLink Specification 113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved	107-110	4	Free Side Device Properties	Free Side Device Properties
- The PCI Express OCuLink Specification 113-117				Used for:
113-117 4 Free Side Device Properties Free Side Device Properties 118 1 Reserved Reserved	111-112	2	Assigned for use by PCI Express	- The PCI Express External Cable Specification
118 1 Reserved Reserved				- The PCI Express OCuLink Specification
	113-117	4	Free Side Device Properties	Free Side Device Properties
119-122 4 Password Change Entry Area Password Change Entry Area	118	1	Reserved	Reserved
	119-122	4	Password Change Entry Area	Password Change Entry Area



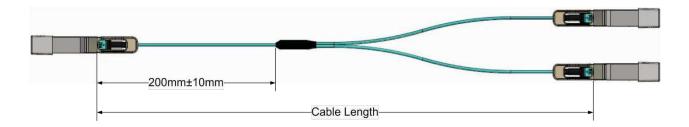
	Password Entry Area Page Select Byte	Password Entry Area			
	,	Page Select Byte			
	Upper Page 00h				
128 1 le	ldentifier	Identifier Type of free side device.(See SFF-8024 Transceiver Management)			
129 1 E	Ext. Identifier	Extended Identifier of free side device. Includes power classes, CLEI codes, CDR capability.			
130 1 0	Connector Type	Code for media connector type. (See SFF-8024 Transceiver Management)			
131-138 8 8	Specification Compliance	Code for electronic or optical compatibility.			
139 1 E	Encoding	Code for serial encoding algorithm. (See SFF-8024 Transceiver Management)			
140 1 5	Signaling rate, nominal	Nominal signaling rate, units of 100 MBd. For rate > 25.4 GBd, set this to FFh and use Byte 222.			
141 1	Extended Rate Select Compliance	Tags for extended rate select compliance.			
142 1 L	Length (SMF)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for SMF fiber in km *. A value of 1 shall be used for reaches from 0 to 1 km.			
143 1 L	Length (OM3 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for EBW 50/125 um fiber (OM3), units of 2 m *			
144 1 L	Length (OM2 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 50/125 um fiber (OM2), units of 1 m *			
145 1	Length (OM1 62.5 um) or Copper Cable Attenuation	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 62.5/125 um fiber (OM1), units of 1 m *, or copper cable attenuation in dB at 25.78 GHz.			
146 1	Length (passive copper or active cable or OM4 50 um)	Length of passive or active cable assembly (units of 1 m) or link length supported at the signaling rate in byte 140 or page 00h byte 222, for OM4 50/125 um fiber (units of 2 m) as indicated by Byte 147. See 6.3.12.			
147 1 [Device technology	Device technology			
148-163 16 V	Vendor name	Free side device vendor name (ASCII)			
164 1 E	Extended Module	Extended Module codes for InfiniBand.			
165-167 3 V	Vendor OUI	Free side device vendor IEEE company ID.			
168-183 16 V	Vendor PN	Part number provided by free side device vendor(ASCII)			
184-185 2 V	Vendor rev	Revision level for part number provided by the vendor(ASCII)			
186-187 2	Wavelength or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5 GHz (Byte 186) and 5.0 GHz (Byte 187)			
188-189 2	Wavelength tolerance or Copper Cable Attenuation	The range of laser wavelength (+/- value) from nominal wavelength. (wavelength Tol. =value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12.9 GHz (Byte 189)			
190 1 N	Max case temp	Maximum case temperature			



191	1	CC_BASE	Check code for base ID fields (Bytes 128-190)
192	1	Link codes	Extended Specification Compliance Codes (See SFF-8024)
193-195	3	Options	Optional features implemented.
196-211	16	Vendor SN	Serial number provided by vendor.(ASCII)
212-219	8	Date Code	Vendor's manufacturing date code.
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any)
220	'	Diagnostic Monitoring Type	in the free side device. Bit 1,0 Reserved.
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the
221	i Emanced Options		free side device.
222	1	CC_EXT	Check code for the Extended ID Fields (Bytes 192-222)
224-255	32	Vendor Specific	Vendor Specific EEPROM



Mechanical Dimension



Note:

- Diameter: 3mm
- Minimum bend radius:30mm
- Cable color:Orange(OM2),Aqua(OM3),Magenta(OM4)
- When L≤1m, the tolerance is +5cm
- When 1m≤L≤4.5m, the tolerance is +15cm
- When 5m≤L≤14.5m, the tolerance is +30cm
- When L≥15m, the tolerance is +2%m

Waring:

- The transceiver optics is supplied with a dust cover. This plug protects the transceiver optics during standard manufacturing processes by preventing contamination from air borne particles. It is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.
- Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment
 is highly recommended. Follow guidelines according to proper ESD procedures.
- Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.



Test Center

1. Performance Testing

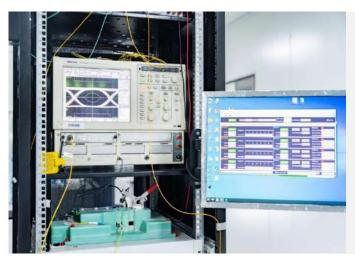
Every fiber optic transceiver is thoroughly tested by the LSOLINK Assurance Program, which is equipped with the world's most advanced analytical equipment to ensure that our transceivers meet the industry's international public protocol standards while still functioning flawlessly in your facility.



Optical Spectrum Inspection

Using the industry's leading optical spectrum analyser to check in real time that the parameters of the optical transceiver's laser comply with industry standards.

- Peak: Peak wavelength and peak level
- > 2nd Peak: Side-mode wavelength and level
- > Mean WI: Center wavelength
- Total Power: Total power of spectrum
- SMSR: Side-Mode Suppression Ratio



Optical Signal Quality Inspection

Using highly efficient sampling oscilloscopes and BERT testers, equipped with an automated test platform to accurately test the signal quality of the transceiver, test records are kept for up to 5 years to ensure the traceability of each transceiver.

- Eye Mask Margin(NRZ)
- > TDECQ(PAM4):transmitter dispersion eye closure
- > OMA: Optical modulation amplitude
- **BER:** Bit error rate
- ER: Extinction Ratio



Flow Pressure Test

Using multi-protocol network traffic analyser with various brands of switches to test the transceiver's ability to transmit at full speed.

- **Bandwidth:** Actual transceiver bandwidth on the port
- Packet Loss
- Packet Errors:CRC Errors/PCS Errors/Symbol Errors
- LinkDown Counts
- > latency

Aboveis part of our test bed network equipment. For more information, Please click <u>download</u> for optical transceiver performance test report.



2. Quality Control

We adopt advanced quality management solutions. Each transceiver is self-inspected, including:20x microscope inspection, 200x microscope inspection, and QC process inspection.



visual inspection



Microscopic inspection: 20X



Microscopic inspection: 200X



Reliability Verification



Optical endface inspection



OQC Inspection



Order Information

Part Number	Length(m)	Connector Type	Cable Type	Cable Jacket
HDR-Q56-2Q-A1	1	QSFP56 to 2xQSFP56	Active Optical	OFNP
HDR-Q56-2Q-A3	3	QSFP56 to 2xQSFP56	Active Optical	OFNP
HDR-Q56-2Q-A5	5	QSFP56 to 2xQSFP56	Active Optical	OFNP
HDR-Q56-2Q-A7	7	QSFP56 to 2xQSFP56	Active Optical	OFNP
HDR-Q56-2Q-A10	10	QSFP56 to 2xQSFP56	Active Optical	OFNP
HDR-Q56-2Q-A15	15	QSFP56 to 2xQSFP56	Active Optical	OFNP



Further Information

Lighting the Path to Global Links

Web | www.lsolink.com

☑ Email | For Sales@lsolink.com

Disclaimer

- We are committed to continuous product improvement and feature upgrades, and the contents cont ained in this manual are subject to change without notice.
- 2. Nothing herein should be construed as constituting an additional warranty.
- LSOLINK assumes no responsibility for the use or reliability of equipment or software not provided by LSOLINK. Copyright LSOLINK.COM All Rights